iW1760

Off-Line Digital Green-Mode Quasi-Resonant PWM Controller

1.0 Features

- No-load power consumption < 50mW at $230V_{AC}$ along with fast dynamic load response and short turn-on delay in typical 20W and above adapter applications
- Primary-side feedback eliminates opto-isolators and simplifies design
- Adaptively controlled soft-start enables fast and smooth start-up for a wide range of capacitive loads (from 330µF to 6,000µF) with output voltage up to 12V
- Tight constant-voltage regulation across line and load range
- Proprietary optimized 79kHz maximum PWM switching frequency with quasi-resonant operation achieves best size, efficiency and common mode noise
- User-configurable 5-level cable drop compensation provides design flexibility
- ***EZ-EMI®*** design enhances manufacturability
- Adaptive multi-mode PWM/PFM control improves efficiency
- No external loop compensation components required
- Built-in single-point fault protections against output short-circuit, output over-voltage, output over-current, and current-sense-resistor-short fault
- Dedicated pins for external over-temperature protection and over-voltage protection, with latch function available
- Tight constant current control enables output current limit and over-load protection
- No audible noise over entire operating range

2.0 Description

The iW1760 is a high performance AC/DC power supply controller which uses digital control technology to build peak current mode PWM flyback power supplies. The device operates in quasi-resonant mode to provide high efficiency along with a number of key built-in protection features while minimizing the external component count, simplifying EMI design and lowering the total bill of material cost. The iW1760 removes the need for secondary feedback circuit while achieving excellent line and load regulation. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions. Pulse-by-pulse waveform analysis allows for a loop response that is much faster than traditional solutions, resulting in improved dynamic load response. The built-in power limit function enables optimized transformer design in universal off-line applications and allows for a wide input voltage range.

iWatt's innovative proprietary technology ensures that power supplies built with the iW1760 can achieve both highest average active efficiency and less than 50mW no-load power consumption in 20W output power range, and have fast yet smooth start-up with a wide range of capacitive loads with output voltage up to 12V, and are ideal for network and monitor adapter applications.

3.0 Applications

- Power adapters for network devices and monitors
- AC/DC power supplies in home appliances
- Universal input AC/DC adapters (15W - 40W)

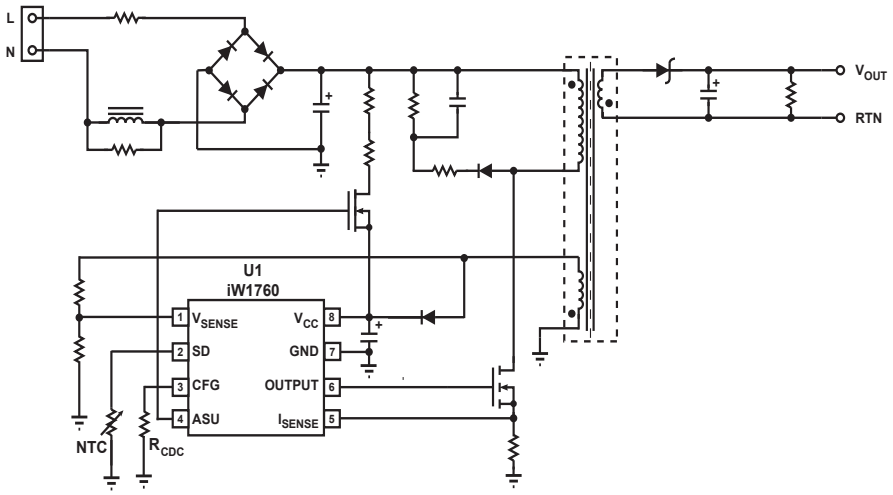


Figure 3.1: iW1760 Typical Application Circuit (Using Depletion Mode N-FET as Active Start-up Device)

(Achieving < 50mW No-load Power Consumption in 20W Adapter Designs)

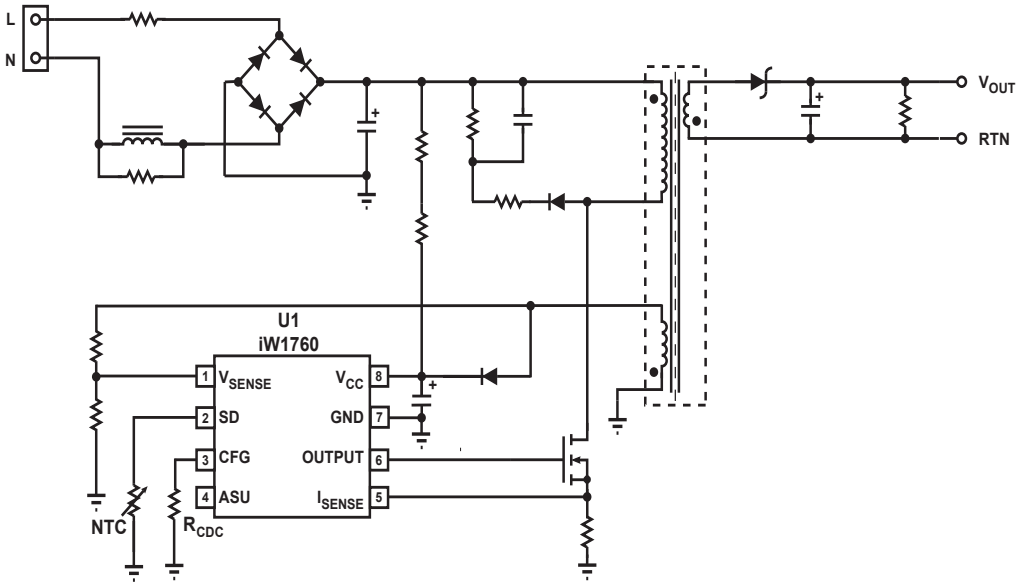


Figure 3.2: iW1760 Typical Application Circuit (Alternative Circuit without Using Active Start-up Device)

Note: Pin 4 (ASU) can be left unconnected if an active start-up device is not needed in the application circuit.

4.0 Pinout Description

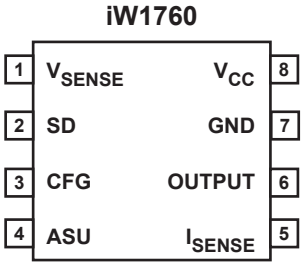


Figure 4.1: 8 Lead SOIC-8 Package

Pin #	Name	Type	Pin Description
1	V_{SENSE}	Analog Input	Auxiliary voltage sense (used for primary regulation).
2	SD	Analog Input	External shutdown control. Used for external over-temperature protection (OTP) by connecting an NTC resistor from this pin to Ground.
3	CFG	Analog Input	Used for external cable drop compensation (CDC) configuration and supplemental over-voltage protection (OVP).
4	ASU	Output	Control signal for active start-up device (BJT or depletion mode NFET).
5	I_{SENSE}	Analog Input	Primary current sense. Used for cycle-by-cycle peak current control and limit.
6	OUTPUT	Output	Gate drive for external MOSFET switch.
7	GND	Ground	Ground.
8	V_{CC}	Power Input	Power supply for control logic.

5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.0.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 8, I_{CC} = 20mA max)	V_{CC}	-0.3 to 18.0	V
Continuous DC supply current at V_{CC} pin (V_{CC} = 15V)	I_{CC}	20	mA
ASU output (pin 4)		-0.3 to 18.0	V
OUTPUT (pin 6)		-0.3 to 18.0	V
V_{SENSE} input (pin 1, I_{Vsense} ≤ 10mA)		-0.7 to 4.0	V
I_{SENSE} input (pin 5)		-0.3 to 4.0	V
SD (pin 2)		-0.3 to 4.0	V
CFG (pin 3, I_{CFG} ≤ 20mA)		-0.8 to 4.0	V
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STG}	–65 to 150	°C
Lead temperature during IR reflow for ≤ 15 seconds	T_{LEAD}	260	°C
Thermal resistance junction-to-ambient	θ_{JA}	160	°C/W
ESD rating per JEDEC JESD22-A114		2,000	V
Latch-up test per JEDEC 78		±100	mA

6.0 Electrical Characteristics

V_{CC} = 12V, -40°C ≤ T_A ≤ +85°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{SENSE} SECTION (Pin 1)						
Input leakage current	I_{BVS}	V_{SENSE} = 2V			1	µA
Nominal voltage threshold	$V_{SENSE(NOM)}$	T_A=25°C, negative edge	1.521	1.536	1.551	V
V_{SENSE}-based output OVP threshold with no CDC compensation (Note 1)	$V_{SENSE(MAX)}$	T_A=25°C, negative edge		1.838		V
I_{SENSE} SECTION (Pin 5)						
Over-current threshold	V_{OCP}		1.11	1.15	1.19	V
I_{SENSE} regulation upper limit (Note 2)	$V_{IPK(HIGH)}$			1.00		V
I_{SENSE} regulation lower limit (Note 2)	$V_{IPK(LOW)}$			0.23		V
Input leakage current	I_{LK}	I_{SENSE} = 1.0V			1	µA

6.0 Electrical Characteristics

V_{CC} = 12V, -40°C ≤ T_A ≤ +85°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SD SECTION (Pin 2)						
Shutdown threshold (falling edge)	$V_{SD-TH(F)}$		0.95	1.0	1.05	V
Shutdown threshold before start-up	$V_{SD-TH(ST\_F)}$		1.14	1.2	1.26	V
Shutdown current source	I_{SD}		95	100	105	µA
CFG SECTION (Pin 3)						
OVP shutdown threshold (rising edge)	$V_{SD-TH(R)}$		0.96	1.015	1.07	V
Input leakage current	I_{BVSD}	V_{SD} = 1.0V			2.5	µA
OUTPUT SECTION (Pin 6)						
Driver pull-down ON-resistance	$R_{DS(ON)PD}$	I_{SINK} = 5mA		16		Ω
Driver pull-up ON-resistance	$R_{DS(ON)PU}$	I_{SOURCE} = 5mA		75		Ω
Rise time (Note 2)	t_R	T_A = 25°C, C_L = 330pF 10% to 90%		104		ns
Fall time (Note 2)	t_F	T_A = 25°C, C_L = 330pF 90% to 10%		14		ns
Switching frequency (Note 3)	f_{SW}	> 50% load		79		kHz
V_{CC} SECTION (Pin 8)						
Maximum operating voltage (Note 2)	$V_{CC(MAX)}$				16	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising	11.0	12.0	13.0	V
Under-voltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling		6.5		V
Latch release threshold	$V_{CC(RLS)}$	V_{CC} falling		4.5		V
Start-up current	$I_{IN(ST)}$	V_{CC} = 10V		6		µA
Quiescent current	I_{CCQ}	C_L = 330pF, V_{SENSE} = 1.5V		4.1		mA
Zener breakdown voltage	V_{ZB}	Zener current = 5mA T_A=25°C	18.5	19.5	20.5	V
ASU SECTION (Pin 4)						
Maximum operating voltage (Note 2)	$V_{ASU(MAX)}$				16	V
Resistance between V_{CC} and ASU	R_{Vcc_ASU}			1100		kΩ

Notes:

Note 1: The V_{SENSE}-based output OVP threshold depends on the CDC setup, see Section 9.12 for more details.

Note 2: These parameters are not 100% tested and guaranteed by design and characterization.

Note 3: Operating frequency varies based on the load conditions, see Section 9.6 for more details.

7.0 Typical Performance Characteristics

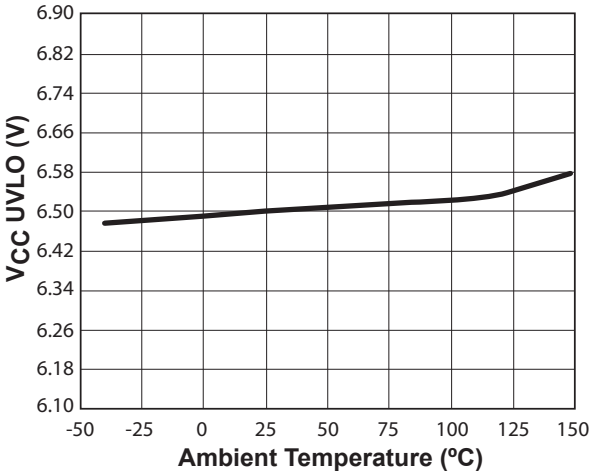


Figure 7.1 : V_{CC} UVLO vs. Temperature

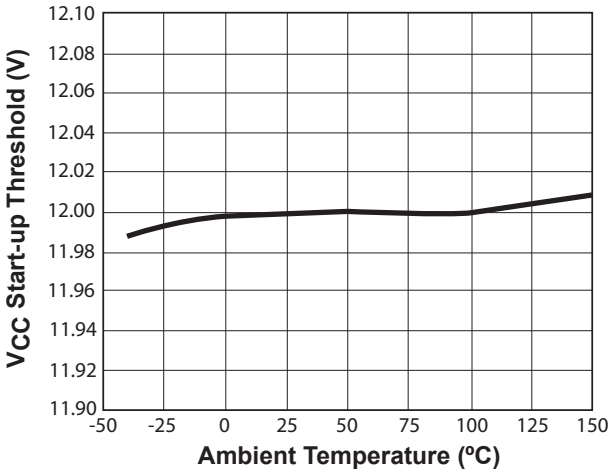


Figure 7.2 : Start-Up Threshold vs. Temperature

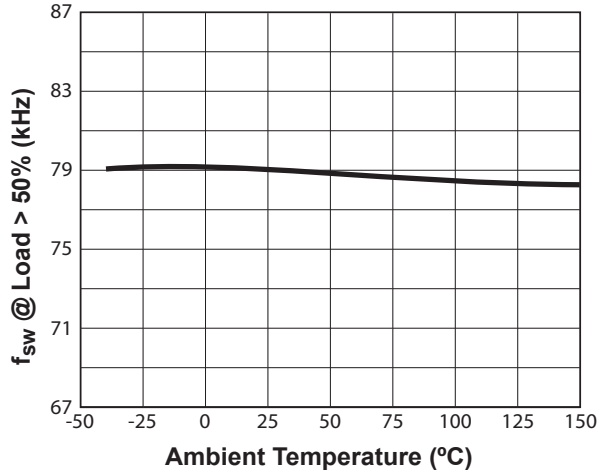


Figure 7.3 : Switching Frequency vs. Temperature[1]

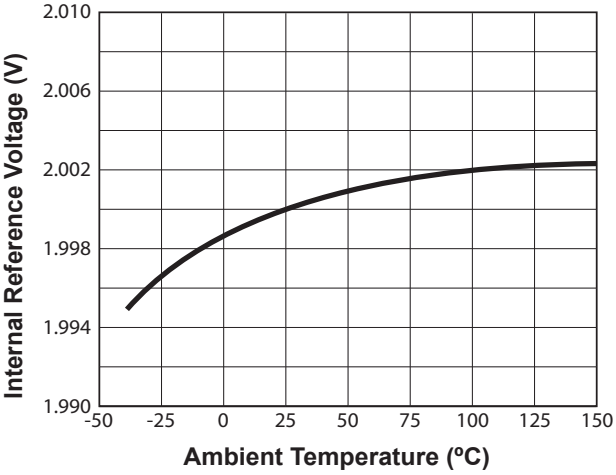


Figure 7.4 : Internal Reference vs. Temperature

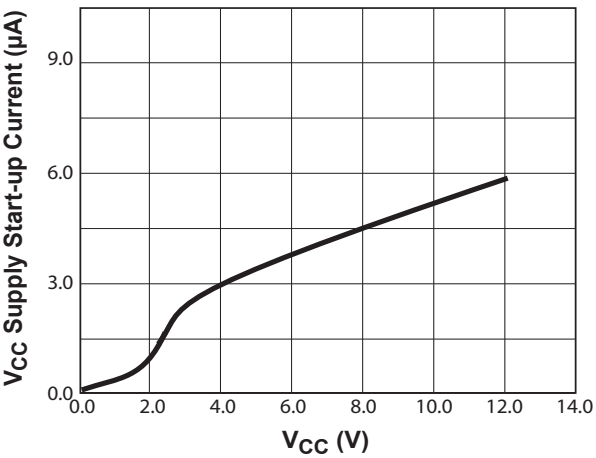


Figure 7.5 : V_{CC} vs. V_{CC} Supply Start-up Current

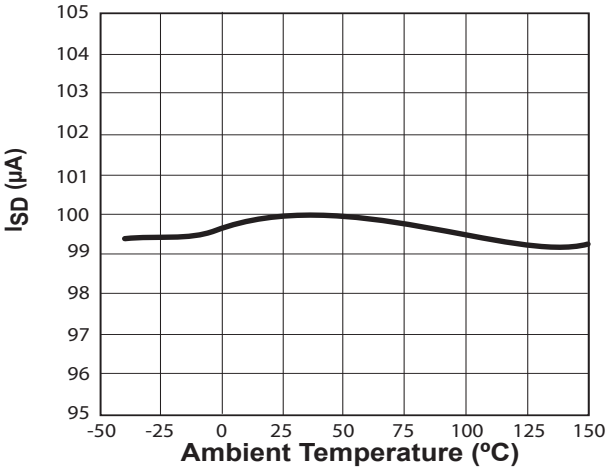


Figure 7.6 : I_{SD} vs. Temperature

Notes:

Note 1. Operating frequency varies based on the load conditions, see Section 9.6 for more details.

8.0 Functional Block Diagram

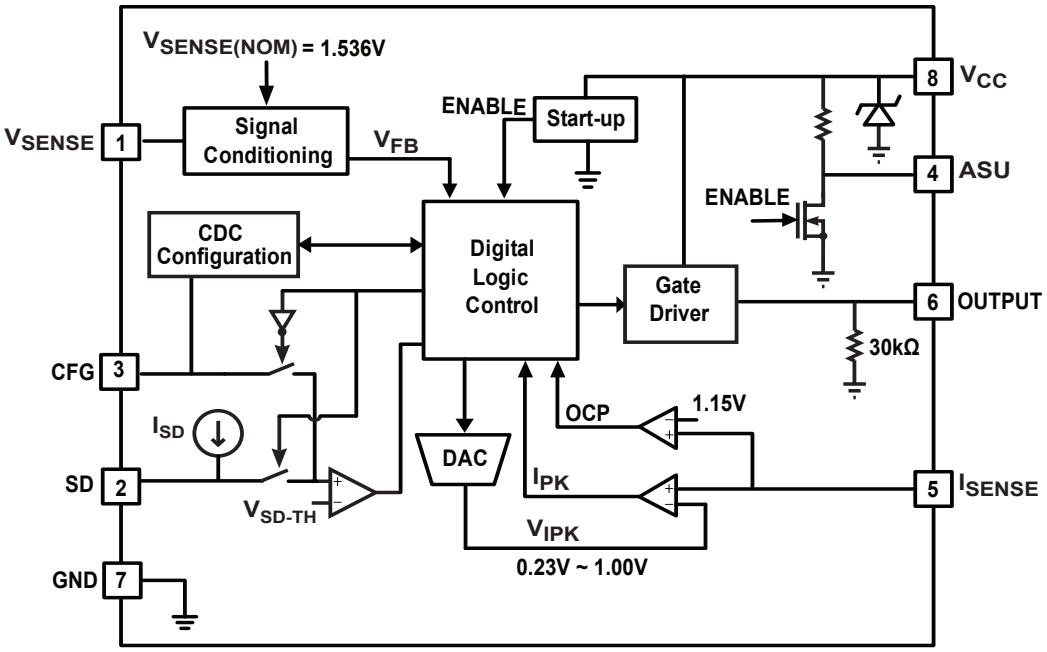


Figure 8.1: iW1760 Functional Block Diagram

9.0 Theory of Operation

The iW1760 is a digital controller which uses a new, proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost solution for low power AC/DC adapters. The core PWM processor uses fixed-frequency Discontinuous Conduction Mode (DCM) operation at higher power levels and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, iWatt's digital control technology enables fast dynamic response, tight output regulation, and full-featured circuit protection with primary-side control.

The block diagram in Figure 8.1 illustrates the iW1760 operating in peak current mode control. The digital logic control block generates the switching on-time and off-time information based on the output voltage and current feedback signal and provides commands to dynamically control the external MOSFET gate voltage. The I_{SENSE} is an analog input configured to sense the primary current in a voltage form. In order to achieve the peak current mode control and cycle-by-cycle current limit, the V_{IPK} sets the threshold for the I_{SENSE} to compare with, and it varies in the range of 0.23V (typical) to 1.00V (typical) under different line and load conditions. The system loop is automatically compensated internally by a digital error amplifier. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation. The iW1760 uses an advanced digital control algorithm to reduce system design time and increase reliability.

Furthermore, accurate secondary constant current operation is achieved without the need for any secondary-side sense and control circuits.

The iW1760 uses adaptive multi-mode PWM/PFM control to dynamically change the MOSFET switching frequency for efficiency, EMI, and power consumption optimization. In addition, it achieves unique MOSFET quasi-resonant switching to further improve efficiency and reduce EMI. Built-in single-point fault protection features include over-voltage protection (OVP), output short-circuit protection (SCP), over-current protection (OCP), and I_{SENSE} fault detection. In particular, it ensures that power supplies built with the iW1760 are best suited for power adapter applications such as wireless routers that have large input capacitances.

iWatt's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as minimum cost, smallest size, and high performance output control.

9.1 Pin Detail

Pin 1 – V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.

Pin 2 – SD

External shutdown control. If the voltage at this pin is lower than 1.2V (typical) at the beginning of start-up or lower than 1.0V(typical) during normal operation, then the IC shuts down. Leave this pin unconnected if the shutdown control is not used (Refer to Section 9.14).

Pin 3 – CFG

Used to configure external cable drop compensation (CDC) at the beginning of start-up and provide over-voltage protection during normal operation by sensing output voltage via auxiliary winding.

Pin 4 – ASU

Control signal for active start-up device. This signal is pulled low after start-up is finished to cut off the active device.

Pin 5 – I_{SENSE}

Primary current sense. Used for cycle-by-cycle peak current control and limit.

Pin 6 – OUTPUT

Gate drive for the external power MOSFET switch.

Pin 7 – GND

Ground.

Pin 8 – V_{CC}

Power supply for the controller during normal operation. The controller starts up when V_{CC} reaches 12.0V (typical), and shuts down when the V_{CC} voltage drops below 6.5V (typical). A decoupling capacitor of 0.1 µF or so should be connected between the V_{CC} pin and GND.

9.2 Active Start-up and Adaptively Controlled Soft-Start

The iW1760 features an innovative proprietary soft-start scheme to achieve fast yet smooth build-up of output voltage with a wide range of output loads, including capacitive loads typically from 330µF to 6,000µF, and for output voltage covering typically from 5V to 12V. In addition, the active start-up schemes enable the shortest possible turn-on delay without sacrificing no-load power loss.

Refer to Figure 3.1 for active start-up circuits using external depletion mode N-FET. Prior to start-up, the ENABLE signal is low, and the ASU pin voltage closely follows the V_{CC} pin voltage, as shown in Figure 9.1. Consequently, the depletion mode N-FET is turned on, allowing the start-up current to charge the V_{CC} bypass capacitor. When the V_{CC} bypass capacitor is charged to a voltage higher than the start-up threshold $V_{CC(ST)}$, the ENABLE signal becomes active and the iW1760 begins to perform initial OTP check (See Section 9.14), followed by CDC configuration (See Section 9.12). Afterwards, the iW1760 commences soft-start function. During the soft-start process, the primary-side peak current is limited cycle-by-cycle by the I_{PEAK} comparator. The whole soft-start process can break down into several stages based on the output voltage levels, which is indirectly sensed by V_{SENSE} signal at the primary side. At different stages, the iW1760 adaptively controls the switching frequency and primary-side peak current so that the output voltage can always build up very fast at the early stages and smoothly transition into the desired regulation voltage at the final stage, regardless of any capacitive and resistive loads that the applications may incur. With a minimum system cost, this adaptively controlled soft-start feature makes the iW1760 ideal in network power adapter applications such as wireless routers in which the adapter needs to drive large capacitive loads with 12V output voltage.

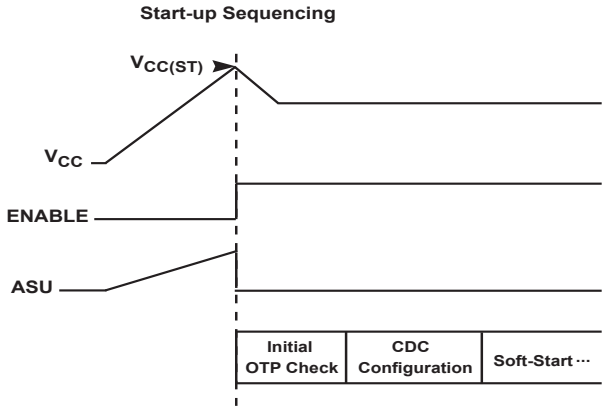


Figure 9.1: Start-up Sequencing Diagram

As the ENABLE signal initiates the soft-start process, it also pulls down the ASU pin voltage at the same time, which turns off the depletion mode N-FET, thus minimizing the no-load standby power consumption.

If at any time the V_{CC} voltage drops below the under-voltage lockout (UVLO) threshold $V_{CC(UVL)}$, then the iW1760 goes to shut-down. At this time the ENABLE signal becomes low, the depletion mode N-FET turns on, and the V_{CC} capacitor begins to charge up again towards the start-up threshold to initiate a new soft-start process.

In applications where the active start-up is not needed, the start-up resistor can be directly connected to the V_{CC} pin without using the active start-up device, and the ASU pin can be left unconnected. Refer to Figure 3.2 for the application circuit.

9.3 Understanding Primary Feedback

Figure 9.2 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D1 is reversely-biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

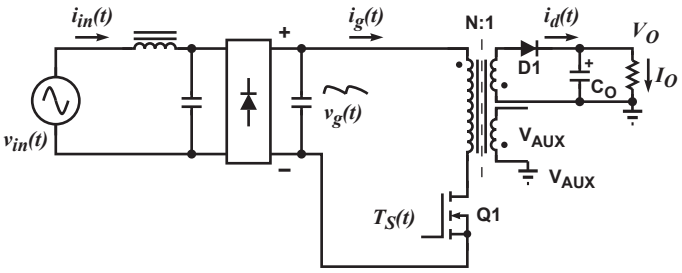


Figure 9.2: Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (9.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \qquad (9.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \qquad (9.3)$$

When Q1 turns off at t_O, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_O, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \qquad (9.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave,

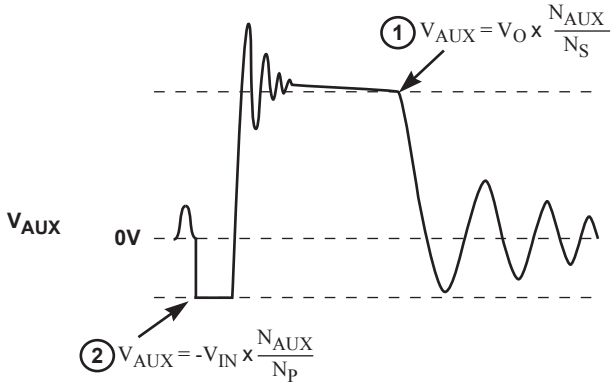


Figure 9.3: Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \qquad (9.5)$$

and reflects the output voltage as shown in Figure 9.3.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV is also small. With the iW1760, ΔV can be ignored.

The real-time waveform analyzer in the iW1760 reads this information cycle by cycle. The device then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

9.4 Constant Voltage Operation

After soft-start has been completed, the digital control block measures the output conditions. It determines output power levels and adjusts the control system according to a light load or heavy load. If this is in the normal range, the device operates in the Constant Voltage (CV) mode, and changes the pulse width (t_{ON}) and off time (t_{OFF}) in order to meet the output voltage regulation requirements.

If no voltage is detected on V_{SENSE} it is assumed that the auxiliary winding of the transformer is either open or shorted and the iW1760 shuts down.

9.5 Current Limit and Constant Current Operation

In overload condition, the iW1760 enters constant current (CC) mode to limit the output current on a cycle-by-cycle basis. In this mode of operation the output current is limited to a constant level regardless of the output voltage, while avoiding continuous conduction mode operation. In case of very heavy loading when the output voltage is low enough, the iW1760 shuts down.

The iW1760 senses the load current indirectly through the primary current, which is detected by the pin I_{SENSE} through a resistor from the MOSFET source to ground.

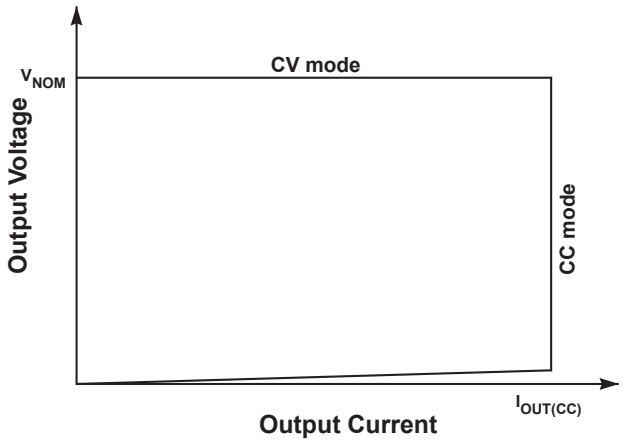


Figure 9.4: Power Envelope

9.6 Multi-Mode PWM/PFM Control and Quasi-Resonant Switching

The iW1760 uses a proprietary adaptive multi-mode PWM / PFM control to dramatically improve the light-load efficiency and the overall average efficiency.

During the constant voltage (CV) operation, the iW1760 normally operates in a pulse-width-modulation (PWM) mode in heavy load conditions. In the PWM mode, the switching frequency keeps around constant. As the output load I_{OUT} is reduced, the on-time t_{ON} is decreased, and the controller adaptively transitions to a pulse-frequency-modulation (PFM) mode. In the PFM mode, the MOSFET is turned on for a set duration under a given instantly-rectified AC input voltage, but its off-time is modulated by the load current. With a decreasing load current, the off-time increases and thus the switching frequency decreases.

When the switching frequency approaches to human ear audio band, the iW1760 transitions to a second level of PWM mode, namely the Deep PWM mode (DPWM). In the DPWM mode, the switching frequency keeps around 22kHz in order to avoid audible noise. As the load current is further reduced, the iW1760 transitions to a second level of PFM mode, namely the Deep PFM mode (DPFM), which can reduce the switching frequency to a very low level. Although the switching frequency drops across the audible frequency range during the DPFM mode, the output current in the power converter has reduced to an insignificant level in the DPWM mode before transitioning to the DPFM mode. Therefore, the power converter practically produces no audible noise, while achieving high efficiency across various load conditions.

As the load current reduces to very low or no-load condition, the iW1760 transitions from the DPFM to the third level of PWM mode, namely the Deep-Deep PWM mode (DDPWM), in which the switching frequency is fixed at around 1.9kHz.

The iW1760 also incorporates a unique proprietary quasi-resonant switching scheme that achieves valley-mode turn-on for every PWM/PFM switching cycle, in all PFM and PWM modes and in both CV and CC operations. This unique feature greatly reduces the switching loss and dv/dt across the entire operating range of the power supply. Due to the nature of quasi-resonant switching, the actual switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI. These innovative digital control architecture and algorithms enable the iW1760 to achieve the highest overall efficiency and lowest EMI, without causing audible noise over entire operating range.

9.7 Less Than 50mW No-Load Power with Fast Load Transient Response

The iW1760 features a distinctive DDPWM control in no-load conditions to help achieve ultra-low no-load power consumption (< 50mW for typical 20W and above applications) and meanwhile to ensure fast dynamic load response. The power supply system designs including the pre-load resistor selection should ensure the power supply can operate in the DDPWM mode under the steady-state no-load condition. If the pre-load resistor is too small, the no-load power consumption increases; on the other hand, if it is too large, the output voltage may increase and even cause over-voltage since the switching frequency is fixed at around 1.9kHz. For typical designs, the pre-load resistor is in the range of 8kΩ to 10kΩ.

In addition to using pre-load resistor, the iW1760 employs a few other features to bring down no-load power consumption. First, the iW1760 implements an intelligent low-power management technique that achieves ultra-low chip operating current at no-load, typically less than 350µA. Second, a low UVLO threshold of 6.5V (typical) enables the power supply system design to have a low V_{CC} voltage at the no-load operation in order to minimize the no-load power. In addition, the active start-up scheme with depletion mode N-FET eliminates the start-up resistor power consumption after the ENABLE signal becomes active.These features combined ensure the lowest system cost power supplies built with the iW1760 can achieve less than 50 mW no-load power consumption at 230V_{AC} input, and very tight constant voltage and constant current regulation over the entire operating range in typical 20W and above compact adapter/ charger applications.

While achieving ultra-low no-load power consumption, the iW1760 implements innovative proprietary digital control technology to intelligently detect any load transient events, and achieve fast dynamic load response for both one-time and repetitive load transients. In particular, for load transients that are demanded in some applications from no-load to full-load, the iW1760 can still maintain a fast enough response to meet the most stringent requirements, with the no-load operating frequency designed at around 1.9kHz.

9.8 Variable Frequency Operation Mode

In each of the switching cycles, the falling edge of V_{SENSE} is checked. If the falling edge of V_{SENSE} is not detected, the off-time is extended until the falling edge of V_{SENSE} is detected. The maximum allowed transformer reset time is 125µs. When the transformer reset time reaches 125µs, the iW1760 shuts off.

9.9 Internal Loop Compensation

The iW1760 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20dB of gain margin.

9.10 Voltage Protection Features

The secondary maximum output DC voltage is limited by the iW1760. When the V_{SENSE} signal exceeds the output OVP threshold at point 1 indicated in Figure 9.3, the iW1760 shuts down.

For this V_{SENSE}-based OVP, latch function is available by product options given in Section 11.0.

The iW1760 protects against input line under-voltage by setting a maximum t_{ON} time. Since output power is proportional to the squared V_{IN} t_{ON} product, then for a given output power, as V_{IN} decreases the t_{ON} increases. Thus by knowing when the maximum t_{ON} time occurs the iW1760 detects that the minimum V_{IN} is reached, and shuts down. The maximum t_{ON} limit is set to 15.5µs. Also, the iW1760 monitors the voltage on the V_{CC} pin and when the voltage on this pin is below UVLO threshold the IC shuts down immediately.

When any of these faults are met the IC remains biased to discharge the V_{CC} supply. Once V_{CC} drops below UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed. For the latched OVP version, the controller can only start up when the fault is removed and input is unplugged to allow V_{CC} to drop 2.0V below UVLO threshold.

9.11 PCL, OCP and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor-short protection (SRSP) are features built into the iW1760. With the I_{SENSE} pin the iW1760 is able to monitor the peak primary current. This allows for cycle-by-cycle peak current control and limit. When the peak primary current multiplied by the I_{SENSE} resistor is greater than 1.15V, over-current is detected and the IC immediately turns off the gate driver until the next cycle. The output driver sends out a switching pulse in the following cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the iW1760 shuts down.

If the I_{SENSE} resistor is shorted, there is a potential danger that over-current condition may not be detected. Thus, the IC is designed to detect this sense-resistor-short fault after start-up and shut down immediately. The V_{CC} is discharged since the IC remains biased. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to start up, but does not fully start up until the fault condition is removed.

9.12 CDC Configuration

The iW1760 incorporates an innovative approach to allow users to configure cable drop compensation (CDC) externally. This configuration is only performed once at the beginning of start-up. It is completed after the initial OTP check but before the soft-start commences. During the CDC configuration, the internal digital control block senses the external resistance value between the CFG pin and ground, and then sets a corresponding CDC level to allow the device to compensate for IR drop in the secondary circuitry during normal operation.

Figure 3.1 shows a simple circuit to set CDC level by connecting a resistor, R_{CDC}, from the CFG pin to ground. The iW1760 provides five levels of CDC configurations: 0, 75mV, 150mV, 300mV, and 450mV, which refer to 5V nominal output voltage. Table 9.1 below shows the resistance range for each of the five CDC levels. In practice, it is recommended to select resistance in the middle of the range wherever possible.

The "Cable Comp" specified in Table 9.1 refers to the voltage increment at PCB end from no-load to full-load conditions in the CV mode, with the assumption that the secondary diode voltage drop can be ignored at the point when the secondary voltage is sensed. Also, the "Cable Comp" is specified based on the nominal output voltage of 5V. For different output voltage, the actual voltage increment needs to be scaled accordingly. For example, for 12V, the corresponding five levels of CDC configurations would be: 0, 180mV, 360 mV, 720mV, and 1080mV.

To calculate the amount of cable compensation needed, take the resistance of the cable and connector and multiply it by the maximum output current.

For each of the CDC levels, the internal V_{SENSE}-based OVP thresholds are different. Table 9.1 also lists the typical OVP thresholds for each CDC level.

9.13 External CFG-Based OVP

In the iW1760, the CFG pin can also be used to provide the external over-voltage protection (OVP) besides fulfilling the CDC configuration. This external CFG-based OVP serves as a supplemental or extra protection in addition to the V_{SENSE}-based OVP. The circuit implementation can be found in Figure 9.5, where two resistors R1 and R2 form a voltage divider to sense output voltage via auxiliary winding, with the tapping point connected to the CFG pin. During the CDC configuration the iW1760 does not send out any drive signal at OUTPUT pin, and the switch Q1 remains in the off state. The resistors R1 and R2 are essentially connected in parallel since the bias winding is virtually shorted. Consequently, the paralleled resistance of R1 and R2 sets the CDC level. Meanwhile, during normal operation, the CFG pin reflects output voltage in real-time, in the similar fashion as the V_{SENSE} does at point 1 in Figure 9.3. The ratio of R1 to R2 sets the external OVP threshold.

The resistance values for the resistor divider, R1 and R2, can be derived as follows.

First, for the given CDC level, the paralleled resistance of R1 and R2 should be within the range listed in Table 9.1:

$$R_{CDC} = \frac{R_1 \times R_2}{R_1 + R_2} \qquad (9.6)$$

Table 9.1: Recommended resistance range and corresponding CDC levels for 5 V output

CDC Level	1	2	3	4	5
R_{CDC} Range (kΩ)	0 ~ 2.20	2.37 ~ 3.21	3.40 ~ 4.64	4.87 ~ 6.65	6.98 ~ X*
Cable Comp (mV)	0	75	150	300	450
V_{SENSE}-based OVP Threshold (V)	1.838	1.861	1.884	1.930	1.976

** The resistance can be as high as 100kΩ, provided CFG pin does not float, which causes device to shut down.*

Second, during normal operation the voltage divider, R1 and R2, sets the desired OVP threshold:

$$(\frac{N_{AUX}}{N_{SEC}}) \times V_{OVP} \times (\frac{R_2}{R_2+R_1}) >= V_{SD\text{-}TH(R)} \quad (9.7)$$

where N_{AUX} is the number of turns for the bias winding, N_{SEC} is the number of turns for the secondary winding, V_{OVP} is the desired OVP tripping point, and $V_{SD\text{-}TH(R)}$ is the internal comparator threshold (1.015V typically) for OVP detection.

The combination of Equations (9.6) and (9.7) leads to

$$R_1 = (\frac{N_{AUX}}{N_{SEC}}) \times R_{CDC} \times (\frac{V_{OVP}}{V_{SD\text{-}TH(R)}})$$
$$R_2 = (\frac{R_1}{R_1 - R_{CDC}}) \times R_{CDC} \quad (9.8)$$

It is recommended the R_{CDC} value is taken as the median value of the resistance range as given in Table 9.1, and R1 and R2 can then be readily derived from Equation (9.8).

It should be noted when the CFG pin is used to provide external OVP, an additional constraint is applied to the resistance range given in Table 9.1. This is because for the OVP configuration in Figure 9.5, a large negative voltage may occur to the auxiliary winding (V_X in Figure 9.5) during the switch on-time, which can cause a negative current flowing out of the CFG pin. Care needs to be taken to ensure R1 and R2 are large enough, so that the resulting negative current is less than the maximum allowed current, specified in Section 5.0.

9.14 External OTP

The iW1760 can be configured to provide external over-temperature protection (OTP) by connecting a Negative-Temperature-Coefficient (NTC) resistor from SD pin to GND. Internally, a 100µA current source is injected to the SD pin, which generates a voltage proportional to the NTC resistance. At high ambient temperatures, the NTC resistance becomes low, which results in a low voltage at the SD pin. If the SD pin voltage drops below an internally-set threshold, then the OTP is triggered, and the iW1760 shuts down.

In the iW1760, the external OTP has a built-in hysteresis by having two thresholds. Before start-up, the OTP is triggered if the SD pin voltage is less than 1.2V; otherwise the device begins the CDC configuration (See Section 9.12), then followed by a normal soft-start process. During normal operation, the OTP threshold is switched to 1.0V, and the device only shuts down when the SD pin voltage is less than 1.0V.

During normal operation, the external OVP and OTP detections alternate every eight cycles. In the eight-cycle duration of OVP detection, the voltage at the CFG pin is fed into the internal comparator's non-inverting input. If the voltage of this pin is above 1.015V at the instant corresponding to point 1 (as indicated in Figure 9.3) for several consecutive cycles, then OVP is triggered. Contrarily, in the external OTP

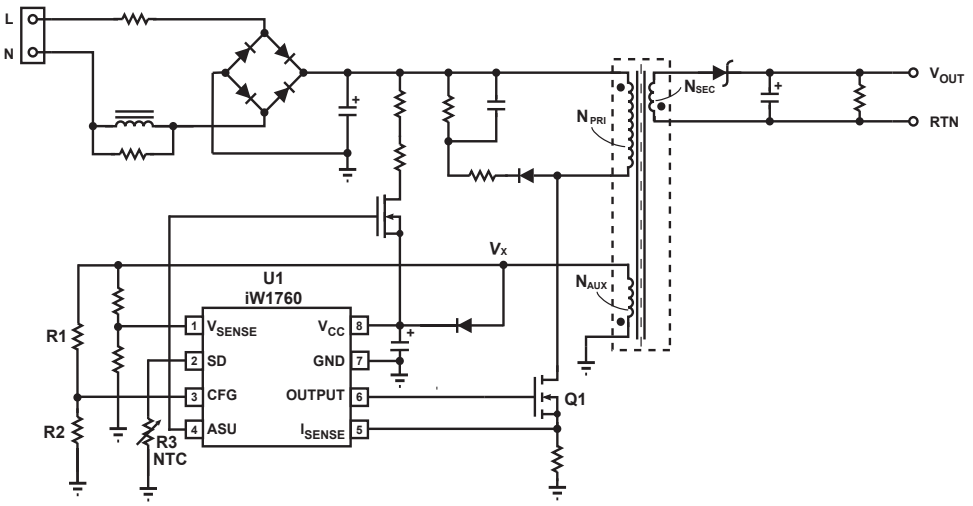


Figure 9.5: Typical Application Circuit with CDC, OVP and OTP Implemented

detection duration, if the voltage at SD pin is below 1.0V for several consecutive cycles, then the OTP is triggered, and the device shuts down.

The SD and CFG pins can be configured to provide different types of applications. Figure 9.6 shows four basic configurations:

In Scheme (a), the CFG pin is directly connected to ground, which sets CDC level to be 1 (i.e. no CDC). On the other side, leaving the SD pin unconnected disables the OTP function.

In Scheme (b), CDC is set to level 1, as in Scheme (a) by grounding the CFG pin. An NTC resistor in paralleled with a capacitor enables the external OTP protection. Note this capacitor is only for decoupling purpose. Its capacitance needs to be less than 47 pF; otherwise the voltage at this pin can cause a prolonged delay and incur unwanted behaviors.

In Scheme (c), a resistor from the CFG pin to ground allows for setting the desired CDC level. Similarly, the NTC resistor enables the external OTP, as it does in Scheme (b).

In Scheme (d), the connections to the CFG and the SD pins are complete as in Figure 9.5, allowing for any level of CDC configuration, and meanwhile enabling the external OTP and OVP.

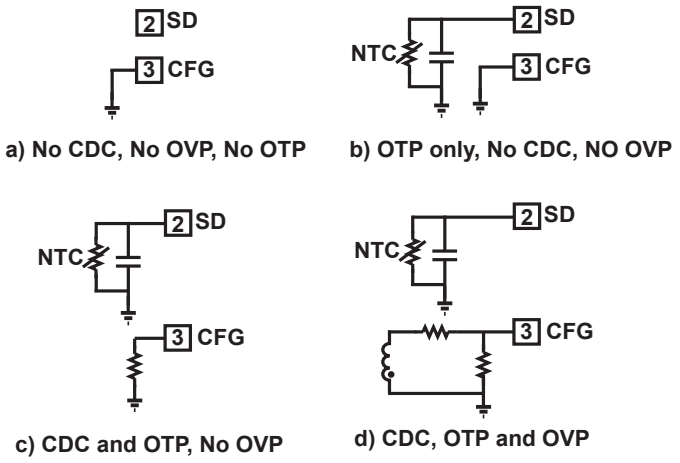


Figure 9.6: CFG and SD Pins Configurations

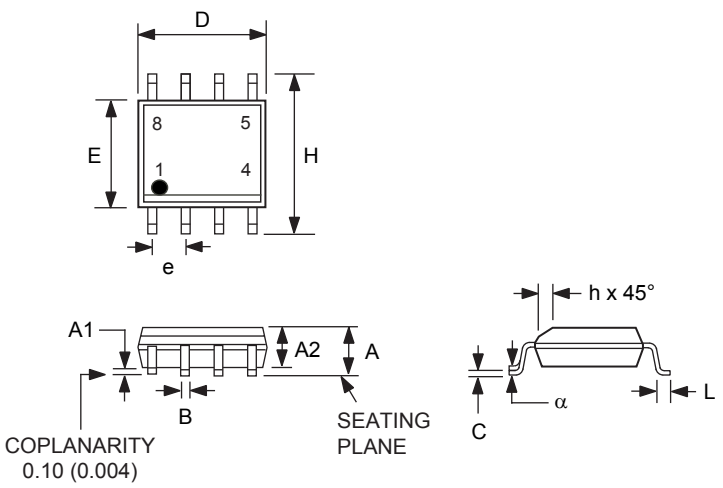
9.15 Latch and Release

In the iW1760, both OTP and OVP (including V_{SENSE}-based and the external CFG-based OVP) can be latched whereby the iW1760 does not attempt to start again even with the fault cleared. In the latch state, the controller recycles itself by periodically ramping V_{CC} up and down between $V_{CC(ST)}$ and $V_{CC(UVL)}$, and the controller does not start up, provided the input stays connected to the AC source. To get out of the latch state, unplugging the input from the AC source is required, so that the V_{CC} is allowed to drop 2.0V below $V_{CC(UVL)}$ to release the latch.

For a fast release, V_{CC} capacitor can be charged directly from the AC source before the diode-bridge rectifier instead of the bulk capacitor. In this way, when the input is unplugged, the V_{CC} capacitor is immediately cut off from the bulk capacitor, allowing for much faster discharging to release the latch, and initiate a normal start-up thereafter.

10.0 Physical Dimensions

8-Lead Small Outline (SOIC) Package



Symbol	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.0040	0.010	0.10	0.25
A2	0.049	0.059	1.25	1.50
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.10	0.020	0.25	0.50
L	0.016	0.049	0.4	1.25
α	0°	8°		

Figure 10.1: Physical dimensions, 8-lead SOIC package

Compliant to JEDEC Standard MS12F

Controlling dimensions are in inches; millimeter dimensions are for reference only

This product is RoHS compliant and Halide free.

Soldering Temperature Resistance:
[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; package can withstand 10 s immersion < 270˚C

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic bocy exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.

11.0 Ordering Information

Part Number	Options	Package	Description
iW1760-00	No OVP/OTP latch	SOIC-8	Tape & Reel[1]
iW1760-01	OVP/OTP latch	SOIC-8	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500 per reel. Minimum ordering quantity is 2,500.

Trademark Information

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